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APPLICAT	ION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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				2189	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

1	Application No.	Applicant(s)					
Office Action Summary	09/846,596	WOUTERS, CORNELIS BERNARDUS ALOYSIUS					
Office Action Summary	Examiner	Art Unit					
	Woo H. Choi	2189					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	36(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. C (35 U.S.C. § 133).					
1) Responsive to communication(s) filed on <u>17 Al</u>	ugust 2005.						
	action is non-final.						
 Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. 							
Disposition of Claims							
4) ☐ Claim(s) 1-3,5-9,11-14 and 16 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-3,5-9,11-14 and 16 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.							
Application Papers	orosion roquiromenii						
9) The specification is objected to by the Examiner.							
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correct	ion is required if the drawing(s) is obj	ected to. See 37 CFR 1.121(d).					
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. §§ 119 and 120							
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list 13) Acknowledgment is made of a claim for domestic since a specific reference was included in the first 37 CFR 1.78. a) The translation of the foreign language pro 14) Acknowledgment is made of a claim for domestic reference was included in the first sentence of the	s have been received. s have been received in Application ity documents have been received in (PCT Rule 17.2(a)). of the certified copies not received c priority under 35 U.S.C. § 119(ext sentence of the specification or visional application has been recomprised to the specification of the specification or the specification of the specificatio	on No ed in this National Stage d. e) (to a provisional application) in an Application Data Sheet. eived. and/or 121 since a specific					
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) D Notice of Informal P	(PTO-413) Paper No(s) atent Application (PTO-152)					

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DETAILED ACTION

Specification

1. The title of the invention is still not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Wear leveling method for flash memory".

Claim Objections

2. Claims 2, 3, 6, 8, 9, 11, and 12 are objected to because of the following informalities:

The claims should be amended to replace "characterized in that" and "characterized by" limitations with "comprising" limitations to make them consistent with their parent claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1 3, 5 9, 11 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assar *et al.* (PCT Publication No. WO 95/10083, hereinafter "Assar").

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5. With respect to claims 1, 7, 13 and 16, Assar discloses a method of data management on a storage medium (figure 6, Flash Memory Device), the storage medium comprising a plurality of blocks in which data can be stored, a first block from said plurality of blocks being selected to execute a mutation on, comprising the steps of:

determining, based on a limit value and a value of a counter associated with the first block, whether a wear level of the first block is acceptable for executing the mutation, and if so, executing the mutation on the first block, and otherwise choosing from said plurality of blocks a second block with a lower wear level than the first block, and copying the data of the second block to the first block (page 16, lines 19 - 29),

wherein each of the blocks has an associated counter for counting the number of mutations in the block that is used as an indicator of the block wear level (figure 10, 620).

However, Assar does not specifically disclose that the limit value is increased when a predetermined number which is at least the majority of the counters of the blocks exceed the limit value. On the other hand Assar discloses a functionally equivalent method where the limit value is effectively increased when a predetermined number which is at least the majority of the counters of the blocks reach a maximum value (page 16, lines 19 – 31) by resetting the counters (see also figure 7, step 238). The limit values in Applicant's and Assar's inventions are used for wear leveling which is a mechanism used to ensure that all blocks are written to or erased fairly evenly. In both inventions, when an erasure count reaches a certain threshold, the data content of the block is swapped with one that is less frequently erased and the block that reached the threshold is not erased until the next wear leveling cycle. When the majority of block erasure

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counters reach the threshold (i.e. wear level is fairly even), the threshold is lifted, or increased, relative to the counters, so that the blocks can be erased (or written to) again and the wear leveling cycle begins anew. In Applicant's invention, the threshold value is increased by increasing the limit value while retaining the counter values. Assar's invention increases this threshold by maintaining the limit value while resetting (or decreasing) the counter values.

The difference between Assar and the claims is the method of increasing the threshold value relative to the counter values to start a new wear leveling cycle. However, this particular method of increasing the limit value while retaining the counter values, as opposed to retaining the limit value while resetting the counter values, does not have a disclosed purpose nor is it disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter of design choice to use the method of increase the threshold value for new wear leveling cycle as opposed to resetting the counter values, since applicant has not disclosed that Applicant's method of increasing the threshold value relative to the counter values (or any other method of increasing the threshold value relative the counter values), overcomes a deficiency in the prior art or is for any stated purpose.

Because a flash cell device has a maximum life in terms of erase-write cycles, there's a need to keep track of the total number of erase cycles to be able to determine the remaining life of a device. One would be motivated to use the method of increasing the limit value while keeping the total counts intact to be able to keep accurate track of the total number of erase cycles on a per block basis for optimal use of all of the blocks. On the other hand, the method of keeping the limit value while resetting the counter has the advantage of having smaller counters using less number of bits and requiring simpler comparison operations. Since the total erase count is reset, the system can easily keep track of the overall wear level by keeping track of the number of wear-level cycle operations, but the total counts for individual blocks are lost.

There are different advantages and disadvantages for each of the methods, with neither one of the methods being non-obvious to one skilled in the art. A flash memory system designer would be motivated to choose one or the other depending on his/her preference and design criteria.

6. Claims 1 – 3, 5 – 9, 11 – 13, and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Assar in view of Bruce *et al.* (US Patent No. 6,000,006, hereinafter "Bruce").

With respect to claims 1, 7, 13 and 16, Assar discloses a method of data management on a storage medium (figure 6, Flash Memory Device), the storage medium comprising a plurality of blocks in which data can be stored, a first block from said plurality of blocks being selected to execute a mutation on, comprising the steps of:

Determining, based on a limit value and a value of a counter associated with the first block, whether a wear level of the first block is acceptable for executing the mutation, and if so, executing the mutation on the first block, and otherwise choosing from said plurality of blocks a second block with a lower wear level than the first block, and copying the data of the second block to the first block (page 16, lines 19 – 29),

wherein each of the blocks has an associated counter for counting the number of mutations in the block that used as an indicator of the block wear level (figure 10, 620).

However, while Assar discloses a functionally equivalent method of increasing the limit value where the limit value is effectively increased when a predetermined number which is at least the majority of the counters of the blocks reach a maximum value (page 16, lines 19 - 31) by resetting the counters (see also figure 7, step 238), Assar does not specifically disclose that the limit value is increased when a predetermined number which is at least the majority of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block. On the other hand, Bruce specifically discloses a method of data management on a storage medium comprising a variety of blocks in which data can be store, where the limit value is increased when a predetermined number which is at least the majority of the counters of the blocks exceed the limit value (abstract, last 4 sentences, col. 9, lines 13 - 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Assar and Bruce before him at the time the invention was made, to use the threshold adjustment teachings of the flash memory storage system of Bruce, in the flash memory storage system of Assar, in order to minimize excess writes to flash memory while re-mapping address to pages of flash memory and be able to use a unified table for re-mapping, wear-leveling, and caching flash memories (Bruce, col. 2, lines 55 – 59).

It also would have been obvious to one of ordinary skill in the art, having the teachings of Assar and Bruce before him at the time the invention was made, to use the threshold adjustment teachings of the flash memory storage system of Bruce, in the flash memory storage system of

Assar, in order to be able to determine the total number of erase/write cycles to a given block of flash memory (Bruce, col. 2, lines 31 - 33). This allows for a more efficient and exact wear-leveling scheme (Bruce col. 2, lines 54 - 55). Assar specifically discloses that periodically clearing the erase counters is undesirable because there is no way to determine the total number of erase/write cycles to a give block of flash memory.

- 7. With respect to claims 2 and 8, the method characterized in that when the value of the counter of the first block is smaller than the limit value, the value of the counter is increased and the mutation is executed, and otherwise a block of which the counter has a lower value than the counter of the first block is chosen as the second block (Assar, page 16, lines 20 25).
- 8. With respect to claims 3 and 9, the method is characterized in that the lower value is the lowest value of the values of the counters of the blocks from said variety (Assar, page 16, lines 22-25).
- 9. With respect to claims 5 and 12, the method further comprises the step of erased the second block after the data of the second block have been copied to the first block (this is inherent in flash memory store as the flash memory cells need to erased before new information can be written).
- 10. With respect to claim 6, the method is characterized in that the mutation comprises erasing the first block (Assar, page 16, lines 22 25).

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With respect to claim 11, the system is characterized in that the system is arranged for initially constructing a table in which the value of the counters of the blocks are stated (Assar, figure 9).

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Assar, or Assar in view of Bruce as applied to claim 1 above, and further in view of Masters (US Patent No. 6,092,160).

Assar and Bruce disclose all of the limitations of the parent claim as discussed above. However, they do not specifically disclose that said copying is preceded by the step of copying to another block any stored data of said first block that is not marked for erasure. On the other hand, Bruce discloses swapping blocks for wear leveling (col. 7, lines 51 – 54). Masters discloses a method of wear-leveling flash memory where copying of less frequently used second block to the more frequently used first block involves swapping the data between the first block and the second block (Masters, figure 5, 512).

Applicants claimed step is a specific sequence in the swapping operation where the content of the first block is temporarily stored in a third location before the content of the second block is copied to the first block, so that the original data in the first block is preserved and copied over to the second block to complete the swapping operation. The use of a third storage location is inherent in a data swapping operation, as a temporary storage location is required to

be able to swap data without losing any information. As to the specific sequence of steps in a swapping operation, one skilled in the art would recognize that there are two ways to perform the swapping operation, just as there are two ways to add two numbers to obtains a sum of two numbers. The first sequence is to copy the first block to a temporary store, copy the second block to the first block, and then copy the original content of the first block from the temporary store to the second block. The second way is to copy the second block to the temporary store, copy the first block to the second block and finally copy the data from the second block from the temporary store to the first block. One skilled in the art would have further recognized that either sequence can be used equally effectively to swap the data, just as adding a first number to a second number is as effective as adding the second number to the first number in obtaining a sum of two numbers.

It also would have been obvious to one of ordinary skill in the art, having the teachings of Assar and Bruce before him at the time the invention was made, to use the data swapping for wear leveling teaching of the flash memory storage system of Masters, in the flash memory storage system of Assar, so that the little worn block becomes heavily used and wear on the heavily worn block is substantially reduced (Masters col. 9, lines 52 - 53).

Response to Amendment

13. The title has been amended to overcome a previous objection. The amended title is still too generic to be indicative of the invention to which the claims are directed. The Examiner asks Applicant to adopt a title similar to the one suggested above.

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14. Claims 1, 3, 5, and 7 have been amended to overcome rejections under 35 USC 112, second paragraph. Corresponding rejections are withdrawn.

Response to Arguments

15. Applicant's arguments filed on August 17, 2005 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation comes from the knowledge generally available to one of ordinary skill in the art. The skill level in the art at the time of invention can be assessed from the prior art references already of record. Desirability of keeping track of the total number of erase/write cycles in a give block of flash memory, because a flash memory cell has a limited life span, was well known prior to the filing date of the instant application as evidenced by Bruce's disclosure (Bruce col. 2, lines 31 - 38). The motivation comes from this prior art knowledge available to one skilled in the art at the time of invention and not from Applicant's disclosure. In fact, Applicant has not even disclosed this particular reason or any other reason for raising the threshold by increasing the limit value. Therefore, the Examiner disagrees with Applicant's

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characterization of the rejection based on Assar as having "used as a blueprint to expand the teachings of Assar without any suggestion or reason for such a expansion."

As to Applicant's argument regarding the rejection based on the combination of Assar and Bruce, again, Applicant's arguments are not persuasive. Applicant states that "Bruce is not proposing to modify Assar. Bruce proposes to replace Assar." Yet, Applicant offers no evidence that Bruce ever made such a proposition. In fact, Assar is not mentioned at all in Bruce's disclosure. Contrary to Applicant's assertion that there is no motivation to combine, the motivation to combine is clearly stated in the rejection and it comes directly from Bruce.

Although Applicant's argument states that there is no motivation to combine, Applicant's real argument seems to be that the two prior art references cannot be combined properly because there are some differences in the way ware leveling is handled in the two teachings and that the proper way to combine is to replace Assar with Bruce. To support this argument, Applicant states "if Assar were to be modified to simply forgo the clearing of erase counters, this would lead to inefficient page thrashing (col. 2, lines 39(40)-42(43))." Applicant also mentions some other differences between Assar and Bruce.

The Examiner disagrees with this assessment for at least two reasons. First of all, Applicant's statement quoted above is simply not true. The erase inhibition feature of Assar (page 16, lines 22 –29) prevents unnecessary swapping, or thrashing, that Bruce mentions. Secondly, the test of obviousness is not what the references teach individually, but what the combined teachings of the references would have suggested to one skilled in the art. There is no basis for Applicant's contention that the combination of Assar with Bruce would result in

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replacement of Assar with Bruce. By definition, a combination of two teachings is not a replacement of one teaching with another. Therefore, for at least the reasons stated above, the Examiner maintains that Applicant has not overcome the prima facie case of obviousness presented in the rejection above.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc

October 27, 2005

BEHZAD JAMES PEIKARI PRIMARY EXAMINER